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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/057,232	01/25/2002	David M. Lewis	306812002500	9737

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EXAMINER	
MALSAWMA, LALRINFAMKIM HMAR	
ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 07/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/057,232	LEWIS ET AL.	
	Examiner	Art Unit	
	Lex Malsawma	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *24-44* is/are allowed.

6)☒ Claim(s) *1-17 and 19-23* is/are rejected.

7)☒ Claim(s) *18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Agrawal et al. (5,490,074; hereinafter, "**Agrawal**").

Regarding Claims 1, 3, 7 and 8:

Agrawal discloses a routing architecture, within a programmable logic device (PLD) of a digital system (i.e., a programmable integrated circuit), to interconnect a plurality of function blocks (including at least a logic array block), comprising:

a plurality of wires (Fig. 1, 4-6) oriented in a first direction (e.g., note in Fig. 5, vertical bus lines 1-4 "V1-V4"), wherein the wires oriented in the first direction have a physical length that is at least substantially the same as an electrically optimum physical length. Note in Col. 6, lines 45-50, Agrawal specifies that the unique architecture "supports efficient utilization of the resources...without speed penalty", i.e., in order for the unique architecture to function without speed penalty, the length of the wires will inherently be substantially the same as an electrically optimum physical length. Therefore, these claims are anticipated. *Specifically regarding Claim 3:* The limitations in this claim have no patentable weight over Agrawal, since Agrawal discloses a physical length that is at least substantially the same as an electrically optimum physical length.

Regarding Claim 2:

Agrawal discloses the routing architecture further comprising a plurality of wires oriented in a second direction (e.g., note in Fig. 5, horizontal bus lines 1-4, "H1-H4"), wherein the physical length of the wires oriented in the first direction (V1-V4) is substantially the same as a physical length of the wires oriented in the second direction (H1-H4), note Figs. 4 and 5. Therefore, this claim is anticipated.

Regarding Claims 4-6:

Agrawal discloses (in Fig. 5) a plurality wires oriented in a second direction (e.g., H5-H9), wherein the physical length of the wires (V1-V4 in Fig. 4) in the first direction substantially differs from a physical length of the wires oriented in the second direction (note in Col. 3, lines 58-60, the long lines "V1-V4" span the entire chip; and in Col. 12, lines 56-61, the bi-directional lines "H5-H9" span two configurable logic blocks, "CLB"). Agrawal further discloses the first direction is orthogonal to the second direction, wherein the first direction and the second direction are vertical and horizontal and directions. Therefore, these claims are anticipated.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various

claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 9-17 and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agrawal (5,490,074) in view of Young (5,818,730).

Regarding Claims 9, 10, 20 and 22:

Agrawal discloses, within a PLD, a two-dimensional routing architecture to interconnect a plurality of function blocks, comprising:

a wire, or first subset (vertical lines 1-4 in Fig. 4) of a plurality of wires, having a first logical length and a physical length, wherein the wire interconnects a subset of the plurality of function blocks (Figs. 1 and 6-8);

a second subset (horizontal lines 1-4 in Fig. 5) of the plurality of wires having a second logical length and a physical length that is substantially the same as the physical length of the first subset of wires;

the first logical length differs from the second logical length. In Figs. 1, 4, 5, and 60, vertical and horizontal long lines "1-4" extend across the entire chip; accordingly, the physical lengths of the vertical and horizontal long lines are substantially the same; and Fig. 60 shows that each CLB has a height longer than its width, therefore, the first (vertical) logical length differs from the second (horizontal) logical length.

Agrawal **lacks** specifying that the physical length of the wire, or the first subset, is substantially the same as an adjustment of the electrically optimum physical length to account for non-electrical considerations or an electrically optimum physical length, wherein the non-electrical considerations include the routing efficiency of the wire at the optimum physical length. Young is **cited primarily to show** that routing efficiency at an electrically optimum physical length would be an obvious feature to implement into a PLD. Young discloses (in Col. 1 lines 39-52) it was well known in the art that routing efficiency of wires is a critical (or at least desirable) aspect of PLD design; and in Col. 5 (lines 18-35), Young specifies one measure of routing efficiency and a means for achieving the routing efficiency, i.e., Young discloses that the highest routing efficiency would be obtained when a wire traverses the largest number of transistors (or in Agrawal's case, the largest number of CLBs). Agrawal discloses the physical length of the wire spans the entire chip (note in Col. 3, lines 58-60, the long lines "V1-V4" span the entire chip), wherein spanning the entire chip would traverse the largest number of CLBs; accordingly, the physical length could be specifically referred to as being substantially the same as an adjustment of the electrically optimum physical length to account for the routing efficiency of the wire at the electrically optimum physical length. In other words, given Young's measure for routing efficiency, it would have been obvious to one of ordinary skill in the art to modify Agrawal by specifically reciting that the wire (or subset of wires) is substantially the same as an adjustment of the electrically optimum physical length to account for the routing efficiency...because Agrawal discloses a most efficient routing for the wire (i.e., V1-V4 span the entire chip, thus traversing the largest number of CLBs), and regardless of whether the wire is actually the electrically optimum physical length, the wire could surely be referred to as being

substantially *an adjustment* of the electrically optimum physical length to account *for the routing efficiency of the wire*, since Young shows that Agrawal's wire is routed in a most efficient manner.

Regarding Claims 11-14:

Agrawal discloses the wire is oriented in a vertical direction (V1-V4, Fig. 4); each of the function blocks is a CLB (i.e., a logic array block); each of the function blocks has a height that differs from it width (note Figs. 56-60 and Col. 38, beginning in line 41)); and a digital system (i.e., a programmable integrated circuit) including the PLD (or CLB, note abstract, lines 1-2).

Regarding Claims 15-17 and 19:

These claims are essentially a method for acquiring the routing architecture of Claims 1, 3, 7, 9, 10 and/or 12, wherein all pertinent limitations within these claims are disclosed (or rendered obvious) by the cited references; therefore, these claims are held obvious over the cited references.

Regarding Claims 21 and 23:

Agrawal discloses the physical length of the first subset (V1-V4, Fig. 4) is substantially the same as the physical length of the second subset (H1-H4, Fig. 5), wherein the first subset is oriented in a first direction (vertical) and the second subset is oriented in a second direction (horizontal).

Allowable Subject Matter

6. Claim18 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claims 24-44 are allowable over the references of record.

8. The following is a statement of reasons for the indication of allowable subject matter:

Claim 18 would be allowable primarily because the references of record, singly or in combination, cannot anticipate or fairly suggest the process for determining the physical length as specified in claim 18, in combination with the method of claim 15.

Claims 24-44 are allowable primarily because the references of record, singly or in combination, cannot anticipate or fairly suggest the PLD specified in claims 24 and 36 including at least four subsets of the plurality of wires; the four subsets having one of three logical length, with the third logical length being shorter than the first logical length; and the third and fourth subsets have equal logical lengths (i.e., have the third logical length) with a physical length of the third subset differing from a physical length of the fourth subset.

Remarks

9. Applicant's remarks/arguments have been carefully reviewed and considered, but they are not persuasive for the following reasons. In general, Applicant asserts that claims 1-17 and 19-23 are allowable over the cited references primarily because the references do not disclose wires having a physical length that is substantially the same as an electrically optimum physical length or an adjustment of the electrically optimum physical length to account for non-electrical

considerations (e.g., see the sentence bridging pages 17-18 in Applicant's remarks). This limitation within the claimed invention has been addressed in detail above, where it has been held obvious over the cited references. In addition to the reasoning provide above, it is noted that Applicant essentially equate electrical optimality with speed optimality (note page 18, last sentence in the first full paragraph); accordingly, a routing architecture which supports efficient utilization of the resources in a CLB array without speed penalty (as specified by Agrawal) indicates that the physical length of the wires would be an electrically optimum physical length, otherwise one must expect to acquire speed penalty in view of Applicant's remarks. In sum, the limitation(s) recited for a physical length of the wires within the claimed invention could be generally applied to any wire within a conventional integrated circuit, especially to the wires disclosed by the Agrawal and Young. In other words, wires with electrically optimum physical lengths are generally desired in the art, and nothing in Agrawal (or Young) indicates that the physical lengths of the wires should not be electrically optimum physical lengths; therefore, the Applicant's remarks are not persuasive.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lex Malsawma whose telephone number is 571-272-1903. The examiner can normally be reached on Mon-Fri (6AM-2PM EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lex Malsawma

July 22, 2004

MATTHEW SMITH
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